ZIP Module V2 Users Manual: DRAFT Version
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Note; This document is just a copy of **ZIP Module V1 Users Manual**, and needs to be updated for the V2 changes. Wayne Johnson (04/10/2001)

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The ZIP module has been designed for experiment E891, the Cold Dark Matter Search (CDMS). The CDMS detector consists of 42 crystals of either pure silicon or pure germanium. Each crystal is approximately one centimeter thick, and 7.5 cemtimeters in diameter. The Germaniun crystals have a mass of approximately 240grams each, while the silicon crystals are on the order of 100 grams each. Each of the crystals has six signal channels; four Phonon sensing and two Charge sensing, and will be operated at a temperature of approximately 0.014 degrees Kelvin.
The primary purpose of a ZIP Module is to provide the interface between a crystal and the data acquisition system for each of the detector's six output signals. The ZIP Module also provides the following inputs to the detector.

QET Bias:	Provides the operating voltage to the QET*, and thus the DC current in the input coil.
Squid Bias:	Provides the SQUID operating current.
LED 1:	Provides a variety of current shapes to LED 1 for freeing trapped charges i the detector crystal.
LED 2	The same as LED 1. Was provided for redundancy.
SQUID Feedback	Amplifies, and conditions the SQUID signal and then sends it to the Feedback coil, in order to cancel the majority of the flux created by the input coil.
FET Heater Pulse	A 30 second pulse sent to a 1Kohm resistor which heats the the two charge channel FETs, prior to the ZIP Module's power-up sequence. This pulse elevates the temperature of the two FETs enough to make them function normally (approximately 70 degrees kelvin).

***Q**uasi-particle-trapping, **E**lectro-thermal-feedback, **T**ransition-edge-sensor

The connections between the detector and the ZIP Module take place via a fifty-pin D-connector located at the upper rear portion of the ZIP Module, and at the E-Stem Breakout-Box on the detector enclosure. The ZIP output signals, being sent to the data acquisition system, leave via a twenty-five-pin D-connector located near the center of the ZIP Module, rear panel.

The design of the 9U ZIP circuitry is based primarily on the design of ten previously built 3U modules. 9U and 3U are the respective sizes of the circuit boards. The ten, 3U modules which were used to design the 9U Zip are as follows; one QET module, four SQUID modules, one DRIVER module, one Qbias module, two Qamp modules, and one FET TEMP module. APPENDIX D is a diagram of the ZIP

module consisting of the connections between the individual 3U modules, in addition to the connections between the ZIP board and the detector. This diagram illustrates of how each 3U module interconnects with the others. While reading these descriptions please refer to fig. 1, or for a more detailed understanding of how each individual circuit operates, please refer to the 9U schematics located on the FERMILAB home page under experiment E891. APPENDIX E is a block diagram of the ZIP Module's sections, portions of this diagram are inserted in this document by the description that it represents.

The ZIP module processes two different types of signals; one signal type is provided by each of the four SQUIDS on each detector, and the other type is provided by the two channels of charge collection circuitry on each detector.

This user's manual is divided up into two sections: **Squid detector electronics** and **Charge detector electronics**. Each section will discuss the function and operation of the associated 3U modules and their subsystems that make up each detector's electronics.

Test points are distributed around this module which are made to accept the Tektronix 5mm scope probes with the Tektronix probe tip (P/N 013-0085-01). These tips have an integral, spring loaded ground lead which is about 3/8" long. This probe tip provides excellent reproduction of fast signals, and only requires two through holes(with the proper spacing) for the two tip leads to contact.

Squid detector electronics

The Squid detector electronics utilizes the basic design of the following 3U modules: Squid module (4), QET module (1), and Driver module (4/6).

QET Specification(Jochen Hellmig, revised 6/7/99)
We have compiled a specification for the CDMSII 9U QET bias. The specification is based on the performance of the most recent Ge-ZIP(Germanium) detectors. The main difference between these kinds of detectors and the previous Si detectors is their lower frequency bandwidth. Therefore, these detectors require better noise performance of the QET bias at lower frequencies (down to ~100 Hz) than the Si detectors. The noise target in V/rtHz terms has changed only slightly compared to the one given to you by Sae Woo Nam. It is now 0.03 μV/rtHz rather than 0.05 μV/rtHz. The relevant frequency range starts at 125 Hz. Which means that the noise of the QET bias should be below 0.03 μV/rtHz for all frequencies above 125 Hz. The Appendix F contains some information on how this specification was derived. The power spectra shown in the figures was measured with a high impedance pre-amplifier and a spectrum analyzer. We didn't use any cold electronics to separate the performance of the board from other noise sources such as SQUIDs. The QET bias board we have tested has shown some microphonics at lower frequencies. I don't know, whether someone has communicated this to you already. I think Dennis Seitz has a pretty good idea of what might be going on. He would also be the person to talk to if you have any further questions regarding this QET bias spec.

QET Description (Mark VanDrunen, revised 5/27/99)
The "Quasiparticle trapping assisted Electrothermal feedback Transition edge sensor"(QET); is also referred to as the "Sensor" is a very specialized circuit mounted on one flat surface of the detector crystal. The detector crystal is either pure Germanium or pure Silicon, approximately 7.5 centimeters in diameter and one centimeter thick. There are four such QETs mounted on one of the flat surfaces of each semiconductor crystal, each covering approximately ¼ of the area of the flat surface. Each of these four sensors consist of 200 superconductors connected in parallel, operating at the critical point, which is right at

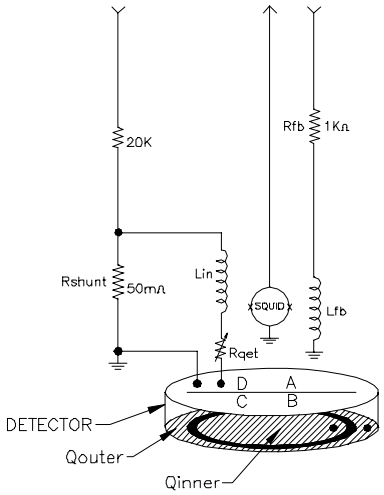


Figure 1: QET diagram

the temperature where a small change in temperature results in a large change in resistance. A WIMP colliding with the nucleus of the Silicon or Germanium crystal loses some energy, which appears as a phonon. This phonon travels to the QET on the surface, causing a small change in temperature, resulting in a large change in the resistance of the QET. The QET is operated in an essentially constant voltage mode. When the resistance, R_{QET}, makes a large change, the current through it makes a corresponding large change. The QET is placed in series with a sensor coil, L_{IN}, which produces a magnetic field in proportion to the current in the QET. A large change in R_{QET} thus results in a large change in the magnetic field produced by L_{IN}. In order to detect this current change a device which is extremely sensitive to magnetic fields is used, this device is known as a SQUID (Super-conducting QUantum Interference Device).

QET Bias Circuitry Description (Mark VanDrunen, revised 5/27/99)
The QET Bias circuitry has the primary purpose of supplying the DC bias voltage to each of the four QETs on the surface of the detector crystal such that the QET remains in the Electrothermal feedback area of operation.

Its secondary purpose is to apply an excessive bias voltage in order to heat the QET sufficiently to force it out a completely superconducting area of operation, should that occur, and back into it's electrothermal feedback area of operation.

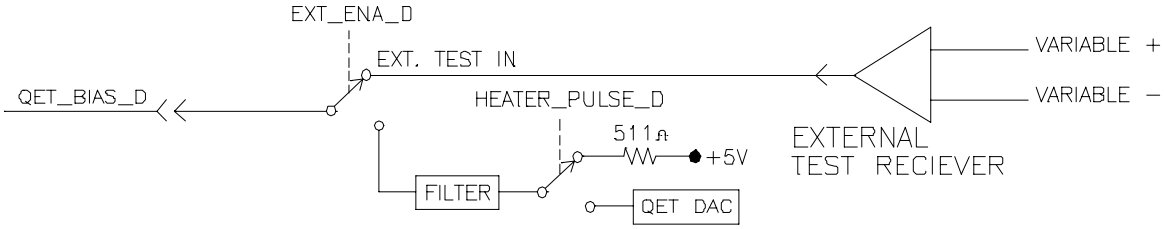


Figure 2: QET Bias diagram

Bias Description (Mark VanDrunen, revised 5/27/99)
The QET Bias circuitry has four outputs, QET_BIAS_A, QET_BIAS_B, QET_BIAS_C and QET_BIAS_D, see schematic sheet 5-1. Each output has the capability of being determined by one of three inputs: EXT_TEST_INPUT, VOLT_LOW_5V, or QET_DAC_X (where X can be A, B, C or D). The selection of the appropriate input is done in two steps. The first step chooses between the QET_DAC_X and the VOLTS_LOW_5V as an input to produce BIAS_X. The second step selects between BIAS_X and the EXT_TEST_INPUT to produce QET_BIAS_X. The QET_DAC_X input has a

range of –5 to +5 Volts DC, with the DAC having a resolution of 12 bits. The EXT_TEST_INPUT is a variable voltage with a source impedance of approximately 5k ohms. The QET_FILTER is in series with the BIAS_X output and adds 5k ohms of resistance to the source impedance for a total output impedance of approximately 10.2k ohms for each QET_BIAS_X output.

The control for the first step is HEATER_PULSE_1, decoded in the logic section as HEATER_PULSE_X (CSR Logic Section). This signal controls the gates of two switches located in U1 (DG413), when the signal is low the switch for QET_DAC_X is closed passing it through as BIAS_X and the switch for VOLT_LOW_5V is opened. When the signal is high then VOLT_LOW_INPUT is passed through as BIAS_X and QET_DAC_X is disconnected.

The control for the second step is EXT_ENA_X. This signal controls two additional switches, also located in U1. When this signal is low then BIAS_X is passed through and is the output QET_BIAS_X, when it is high then the EXT_TEST_INPUT signal (EXT_TEST_RECEIVER Section) is passed through to become QET_BIAS_X. QET_BIAS_X is then sent through the 25 pin backplane connector, to the detector via a 25 conductor cable. The following truth table shows the relationship of the input controls and the output signal.

EXT_ENA_X	HEATER_PULSE	OUTPUT
0	0	QET_DAC_1
0	1	VOLT_LOW_5V
1	X	EXT_TEST_INPUT
Note: X= Don't Care		

Heating Pulse Description (Mark VanDrunen, revised 5/27/99)
+5 Volts is applied as a pulse of power to heat the QET and is controlled by the HEATER-PULSE signal, which is decoded in the CSR logic section. The function of the heater pulse is to return the QET to the electrothermal feedback area of operation, in the event it were to become completely superconducting. When completely superconducting, the QET has become cold enough to have no resistance and dissipates no power, as a result, the Electrothermal Feedback mechanism ceases to function. Applying +5V pulses to the QET heats it up and forces it out of the completely superconducting area of operation and into the electrothermal feedback area of operation. The heater pulse is fixed at 100 milliseconds. When the heater pulse is active the output impedance of QET_BIAS_X is reduced from approximately 10.2k ohms to approximately 5.1k ohms.

SQUID Module Description (Merle Haldeman, revised 5/7/99)
The SQUID Module was designed to receive signals from the SQUID (Superconducting Quantum Interference Device) near the detectors. SQUIDs consist of an arrangement of super-conducting, josephson juntions that can quite easily measure a single quantum of magnetic flux (200 nanogauss-cm^2), and voltages as small as 10 fempto volts.

The SQUID Module circuitry consists of the following subcircuits; Squid Front End, Squid Variable Gain Amplifier, SQUID Feedback Integrator, SQUID Feedback Polarity Selection, Squid Feedback Monitor, Squid Feedback Logic and Squid Zap Control, descriptions of which follow.

SQUID Front End (Tom Crenna, revised 5/11/99)
The Squid Front End does two things, it sends a bias voltage to the SQUID for proper operation and it receives the output signal (SQUID_SIG) of the Squid. The SQUID bias voltage is sent directly to the SQUID via a 20kΩ resistor (R7). The signal from the SQUID passes through a relay (U1: Teledyne,712 DPDT relay) to the non-inverting input of an amplifier (U2: AD797) where it is amplified and appears as AMP_OUT. The AD797 is an ultralow distortion, ultralow noise op-amp, being used as a preamplifier to provide a gain of approximately 16.4. The SQUID bias voltage is present at the amplifier input with the SQUID signal superimposed on it. The SQUID_BIAS voltage is controlled by the SQUID_BIAS_DAC.

In order to compensate for the bias voltage at the input of the amplifier, there is another input, LOCK_POINT_ADJ, coming from the SQUID_LOCKPNT_DAC that goes to the inverting input of the amplifier, via R4. This input creates the proper offset to compensate for the SQUID_BIAS voltage. During the time the relay(U1) is passing the SQUID signal to amplifier U2, the SQUID ZAP circuitry capacitor is being charged or being held in a charged state. For an explanation of the ZAP circuitry, see SQUID ZAP control.

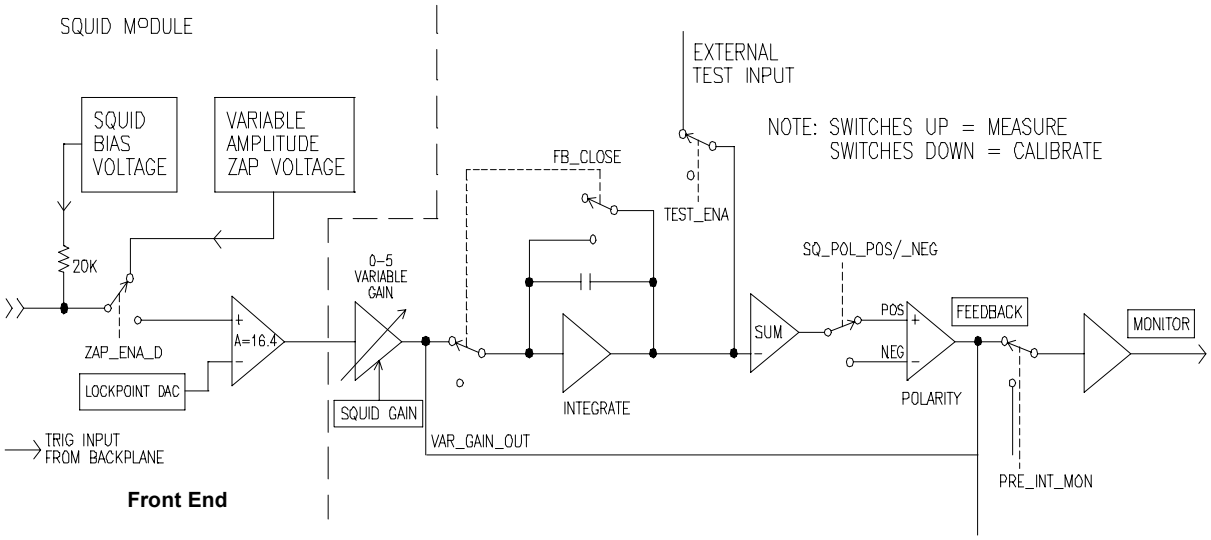


Figure 3: Squid Module diagram

SQUID ZAP Control (Tom Jankovsky, revised 5/26/99)

The purpose of the SQUID ZAP control (schematic 4-1) is to issue a pulsed voltage to the squid, the amplitude of the voltage is determined by the ZAP DAC output. This voltage is sent to the SQUID portion of the detector causing it to heat up. Heating of the SQUID pushes it out of the super conductive region making the Josephson Junctions resistive. This resistance dissipates trapped flux lines as heat. The voltage is provided by discharging the Zap Capacitor (C5: 0.022F capacitor) that has been charged to a voltage set by the output of the ZAP DAC. Discharging of the capacitor is controlled by the ZAP_ENA_A signal. The ZAP_ENA_A signal is a 2 second pulse that controls the discharge time of the Zap Capacitor onto the SQUID. The 2 second input pulse is sent from the CSR logic section via control lines: ZAP_ENA_A, ZAP_ENA _B, ZAP_ENA _C, ZAP_ENA_ D. The ZAP_ENA_A signal is Exclusively ORed with Front End ground so that when it is LOW, a LOW is produced at the output of the Exclusive OR gate (U5: CD4070BCM). This LOW signal turns the FET switch (U1 & U2: mtdf1p02hd) 'on', energizing the relay (U1, schematic sheet 3-2) in the SQUID front-end section. While the relay is energized, the zap capacitor discharges into the SQUID portion of the detector, causing the trapped flux to dissipate. When the relay is not energized, the zap capacitor is being charged via the ZAP_V line. The ZAP_V line is supplied by a special op-amp (U4: LT1363CS8) capable of driving highly capacitive loads. The input of the op-amp is supplied by the ZAP_ DAC output.

The Sense Bias CSR in the logic circuitry is responsible for decoding the setting of the bits that enable the zap control for each of the SQUIDS, see Chart 1, Part 2: CSR Subsection Outputs vs. Data Buss Bits, for data bit assignment versus SQUID. Once the SQUID's zap enable bit has been set high, then the zap pulse is executed by one of two different methods. One method for executing the zap pulse is to 'Write' to the Test Pulse address XXFF, where XX is the slot number that the Zip Module is located in (see Chart 1, Part 1: Section, Subsection Decoding). When the Test Pulse is written to, all SQUIDs that have their Zap enable set high will receive a zap pulse at the same time. The second method is done in two steps. The first step is to set the TRIG_ENA bit high. The TRIG_ENA signal is data bit 0 of CSR5, see Chart 1, Parts 1 and 2. The second step is for the user to generate a TRIGPLUS_MINUS signal on the backplane of the electronics crate. The TRIGPLUS_MINUS signal is an output of the Auxiliary card that is mounted in slot

21 of the electronics crate. The TRIGPLUS_MINUS signal will trigger a zap pulse to ALL SQUIDs, connected any Zip module in the electronics crate, that have had their zap enable set high.

SQUID Variable Gain Amplifier (Tom Crenna, revised 5/21/99)

The squid variable gain amplifier (schematic sheet 3-3) provides a gain of 0 to -5, and is proportional to the squid gain DAC setting, i.e., -5 volts out of the DAC provides a gain of -5. The gain is applied to the output of the SQUID front-end amplifier, U2. This variable gain amplifier utilizes a matched pair of N-channel JFET's (Q1), to control the gain, by utilizing them as variable resistors. One JFET is used with U2 in a feedback loop, strictly to control it's R_{DS}. The other JFET, assuming it has a similar R_{DS}, sets the gain of U1, with the gain being equal to the negative of the ratio, R_{13}/ R_{DS}.

The top FET and U2 circuitry operate as a current controlled resistance. Any current ($I_{control}$) pulled from the junction of pin 1(source) of the FET and pin 2(inverting input) of U2 must be supplied by the +100mV source. This is because the input impedance of U2 pin 2 is very high and will not source or sink $I_{control}$. As a result, U2 drives pin 3(gate) of the FET to source or sink $I_{control}$. This is necessary in order to keep pin 2 of U2 near zero volts. If we were to sink 0.5mA from the junction of JFET pin 1 and U2 pin 2, U2 would drive pin 3 of the FET with a voltage which would make the FET conduct the 0.5mA from the 100mV regulator. This requires that R_{DS} have a value of 200 ohms. R_{DS} then is determined by 100 mV/ $I_{control}$. $I_{control}$ is determined by V_{DAC}/6k ohm). The JFET's are enclosed in a single package to minimize parasitic effects, and improve matching between the pair. The 100mV regulator (U3: OPA27) provides the drain to source voltage that is large enough to be easily regulated, and low enough to control R_{DS} with voltage across it in the range of what the signals may produce across the paired JFET in the signal path. The bottom and top sections of Q1 have the same drain to source resistance due to the matched characteristics of the JFET pair. The bottom section of Q1 is used as the input resistance to the inverting amplifier (U1: CLC409AJE). Therefore, the gain of U1 is determined by the standard relationship of an inverting amplifier, A = -(Rf / Rin) where Rf is R13 and Rin is R_{DS}. The internal resistance of Q1 will vary between approximately 120 ohms when V_{DAC} is equal to –5 volts, and infinity when V_{DAC} is equal to zero volts. The final gain is then determined by:

$A = (R_{13}/ R_{DS}) = (VDAC \times 604 \text{ ohms}/100mV \times (1k \text{ ohm} + 4.99k \text{ ohm})) = VDAC$

JFET (U440) operating point characteristics:

The family of curves for the Temic U440, JFET used in the squid variable gain amplifier, are shown below in figure 4. The curves were produced using ORCAD SPICE for the U440 library model. These curves were produced by sweeping the drain to source voltage while incrementing the gate to source voltage for each sweep. The drain to source voltage was swept from -150 to 150mV and the gate to source voltage was incremented from 0 to –2.8V, in 0.2 volt steps. The vertical axis represents the drain current and the horizontal axis represents the drain to source voltage. Each line represents a different gate to source voltage as the drain to source voltage is varied. The +/- 150mV sweep value was used because the actual circuit application is expected to be in that range. The slope of the lines in figure 4, provide the drain to source resistance. For a drain to source voltage of +/-150mV, and gate to source voltage of 0V, the resultant drain current is approximately 1.6mA, giving a resistance R_{ds} of 150mV/1.6mA = 94Ω. If the magnitude of gate to source voltage is increased in the negative direction, the slope of the resultant curve will decrease, providing and increased R_{ds}. This feature of the JFET is what allows us to use it as a voltage controlled, variable resistor.

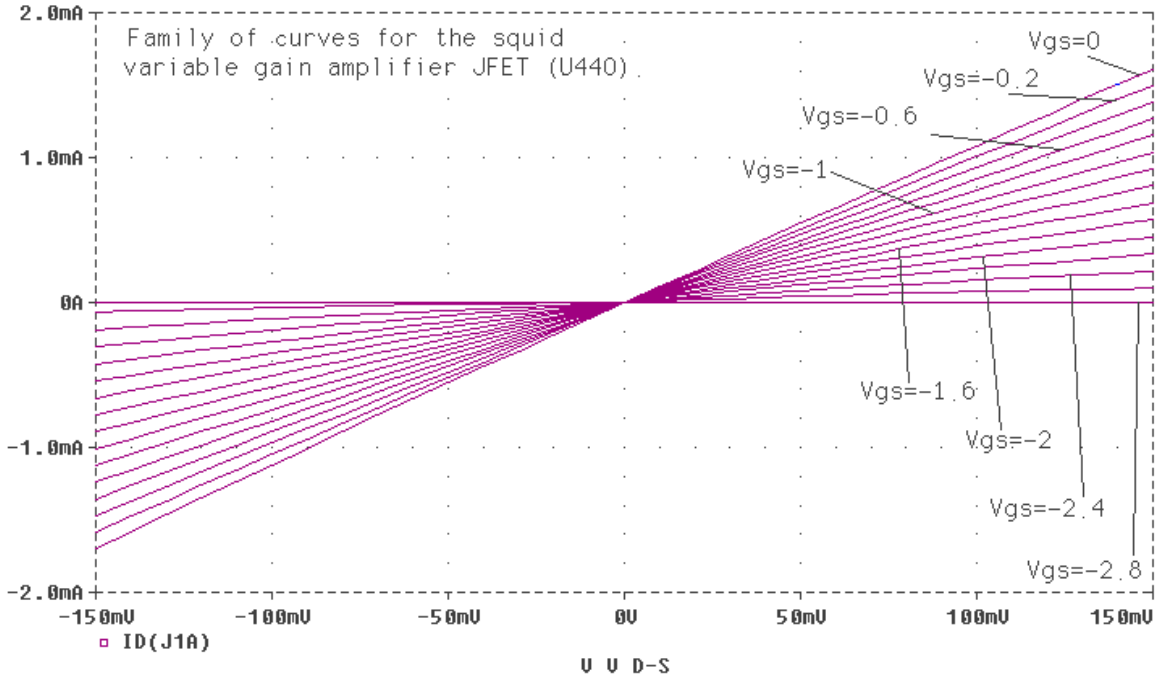


Figure 4: JFET characteristics curve

SQUID Feedback Integrator (Merle Haldeman 3/17/00)

The integrator used on this module is switched into, or out of the circuit with insulated-gate FETs (U3 and U4) being utilized as switches. The basic integrator consists of R38, the right half of U5 (the left half is there to increase the integrator's open loop gain) and the feedback capacitor (C34 and C35). The transfer function is:

$$V_o = \frac{1}{RC}\int V_{in} \bullet dt \,.$$

Where;

V_o is the voltage at U5 pin 1
R is R38
C is C34 plus C35
V_{in} is the voltage on the drain of U3

U3 and U4 function as switches, which are complementary, i.e., when U3 is open, U4 is closed and visa versa. Opening U3 disconnects the input signal (V_{in}) to the integrator, taking it out of the phonon sensor feedback loop. During this time U4 is closed discharging the integrating capacitor (C34 and C35), causing the output of the integrator (V_o) to remain at near zero. When U3 is closed and U4 is open, the integrator is in the phonon sensor feedback loop, and functions as an integrator.

The control voltage at the gates of U3 and U4 couple charge through the parasitic capacitances of U3 and U4, to the input of the integrator. This parasitic charge results in an initial offset on the integrating capacitance. This parasitic charge is neutralized by the charge coupled through C1. C1 thus needs to be adjusted for zero offset at the output of the integrator, when the integrator is connected into the feedback loop. Resistor R33 limits the low frequency gainof the integrator to approximately 70. The combination of the integrating capacitance and R33 cause the gain of the integrator to be 3dB down at approximately 2.4 kHz.

SQUID Feedback Polarity Selection (Tom Jankovsky, revised 6/01/99)
The SQUID polarity stage allows the user to change the polarity of the SQUID summing amplifier output signal, SUM_AMP_OUT, see schematic sheet 3-6. Activating either the SQUID_POL_NEG or SQUID_POL_POS line changes the corresponding polarity of the output to negative or positive. These signals accomplish polarity reversal by utilizing a latching relay (U11: Teledyne Relay 722) that routes the SUM_AMP_OUT signal to the inverting input of the amplifier (U10: CLC402AJE) for negative polarity, or to the non-inverting input for positive polarity. The output signal, FEEDBACK, leaving the polarity section is connected to the Squid feedback monitor and also out the backplane to the detector.

Squid Feedback Monitor (Mark Van Drunen, revised 6/01/99)
The squid feedback monitor selection circuitry, see schematic sheet 3-7, acts as a two-pole-single-throw switch which allows either the FEEDBACK signal (from the polarity section) or the V_GAIN_OUT signal (from the squid variable gain amplifier section) to pass through their appropriate amplifiers and become the output, MONITOR. The CLC410AJE (U7, U8) is a low noise, current feedback amplifier which has a fast disable/enable control, enabling the amplifier output when the control is high, and disabling the amplifier output when the control is low. The signal coming from the enabled amplifier is called the MONITOR signal, and is sent to the appropriate SQUID driver section.
The FEEDBACK signal is passed through the op-amp (U8) to the driver section only when FEEDBACK_SEL is set HIGH by the Squid Feedback Logic Section. This is controlled by the PRE_INT_MON signal from the Squid CSR (control status register)(U105:CYC37256). Pins 2,3,4, and 5 of U105 are the four PRE_INT_MON lines for the four squids. See Zip Module Addressing section for a description of CSR selecting.
The V_GAIN_OUT signal is passed through the op-amp (U7) to the driver section only when V_GAIN_OUT_SEL is high. V_GAIN_OUT_SEL is sent from the Squid Feedback Logic Section. This is controlled indirectly by the same pins on the CSR that control FEEDBACK_SEL. When FEEDBACK_SEL is sent a high from the PRE_INT_MON line the V_GAIN_OUT_SEL is at ground and visa versa. Thus the PRE_INT_MON signal controls both FEEDBACK and V_GAIN_OUT.

SQUID Feedback Logic (Mark Van Drunen, revised 6/01/99)
The Squid Feedback Logic (schematic sheet 3-8) allows the user to choose whether or not, the V_GAIN_OUT signal (schematic sheet 3-5) will pass through the integrator (U5:CLC428AJE). This is accomplished turning a FET SWITCH 'on' or 'off'. Plus 5 volts on the gate turns the FET SWITCH 'on' and minus 5 volts on the gate turns the FET SWITCH 'off'. If the user chooses not to let the V_GAIN_OUT signal pass through the integrator then FET SWITCH U3 is turned 'off' and FET SWITCH U4 is turned 'on'. The circuitry on schematic sheet 3-8 provides the level shifting required between the Squid CSR and the gate of the FET SWITCH. The FB_CLOSE_SQ outputs of the Squid CSR turn the FET switches 'on' and 'off'.

The Squid Feedback Logic is controlled by one of the FB_CLOSE_SQ signals sent from pins 124, 125, 126, and 127 of U105 in the CSR Logic Section. If FB_CLOSE_SQ arrives at the base of the Level Translator (pin 1) of Q1 (MMBT4403LTI) as a high level, Q1 is off and the collector (pin 3) should be at –5 volts. On the other hand, a low at the base of Q1 results in Q1 being turned on hard, and the collector will be at approximately +5 volts. The collector level then goes into an Exclusive-OR Gate (U1: CD4070BCM, CMOS Quad, Dual input). If the inputs of the exclusive-or gate are equal the gate outputs a low level, if the inputs are different it outputs a high level. Three output signals (FET_A, TRIM_CAP, and FET_B) are used to control the Squid's integrator. The integrator is not used if FB_CLOSE_SQ is high, the FET_A output and the TRIM_CAP output are high and the FET_B output is low. When the integrator is not used, the capacitance in the feedback loop is discharged by turning 'on' FET SWITCH U4 (FET_B), and the V_GAIN_OUT input signal is blocked by turning 'off' FET SWITCH U3 (FET_A). When FB_CLOSE_SQ is low, the two FET SWITCHES change state and the integrator integrates the V_GAIN_OUT signal

Driver Description (Andy Paullin, revised 6/02/99)
The Driver(schematic sheet 10-1) circuitry, of which there are six independent, analog channels, each of which has a selectable gain and polarity, as well as controllable DC input offset voltage. The gain choices are 1, 1.43, 2, 5, 10, 14.3, 20, and 50, and the polarity can be inverting or non-inverting for any gain setting. The 3dB bandwidth of each channel is approximately 1 MHz wide. Offset is controlled at the input, and as a result, is unaffected by the gain and visa-versa. The input offset is adjustable over a range of -5 to +5 volts, in approximately 2.44millivolt steps. Each channel is designed to drive a 50 ohm load with shunt capacitance of up to 1000pf. A Driver is utilized in each of the four SQUID channels, as well as the two Qamp channels. The SQUID and Qamp output signals are processed via the Driver and sent to the data acquisition system for analysis.

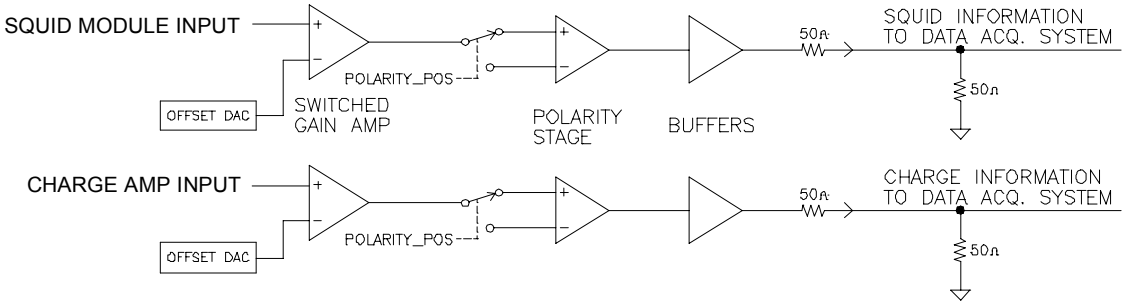


Figure 5: Driver Module diagram

The gain and polarity for each driver channel is controlled by a combination of latching relays (U1, U2, U3, U4: DS2E-ML2-DC12V). This type of relay requires power only during the transition time that the relay is changing state (approximately 12 milliseconds), the remainder of the time the relay coil is disconnected from power with one end of the coil grounded. The input of each driver channel consists of a pseudo instrumentation amplifier (U9, U10: AD829JR and U13: OPA627GU). U9 and U10 make up the input stage, which has a differential input and a differential output. The output of the Squid Module, MONITOR is inputted into U9, and the output of OFFSET_DAC is inputted into U10, which is subtracted from the input signal. The outputs of U9 and U10 are converted to a single ended output by U13. However, U13 is incapable of driving a 50 ohm load, and is thus it's output is buffered (U14: BUF634F). The feedback for U13 includes the output of U14 in order to minimize additional gain and offset errors introduced by U14.

The gain of the first stage is 20 when the two 6.8k ohm resistors (R1, R2) are switched in by U4, or a gain of 2 when the two 357 ohm resistors (R16, R17) are switched in by U4. The gain of the second stage is 5 when only the 5k ohm resistors (R25, R26) are in the feedback circuitry. The second stage gain is 2 when the 3.32k ohm resistors (R27, R28) are placed in parallel with the 5k ohm resistors by U3. The second stage gain is 1.43 when the 2k ohm resistors (R29, R30) are placed in parallel with the 5k ohm resistors by U1. The second stage gain is 1 when all three resistors, 5k, 3.32k and 2k, are placed in parallel by U1 and U3. The actual gain of the driver is one half of the combination of the first and second stage gains, because of the 49.9 ohm resistor (R15) that is in series with the output of U14 which is driving a 50 ohm load. Table B on schematic sheet 10-1 shows the relationship of the relay settings to the output gain of the driver module.

The polarity of the driver output is determined by the setting of U2. When relay U2 is set by the control input of POLARITY_POS, the output of U9 is routed to the non-inverting input of U3 and the output of U10 is routed to the inverting input of U3 resulting in a non-inverted output from the driver. When U2 is controlled by the POLARITY_NEG input, the output of U9 is routed to the inverting input of U3 and the output of U10 is routed to the non-inverting input of U3 resulting in an inverted output from the driver. Table A on schematic sheet 10-1 shows the relationship of the relay settings to the polarity of the output.

Charge detector electronics

The Charge detector electronics utilize the following 3U modules: Q amp module (2), Q bias module (1), LED module (1), FET temp module (1) and Driver module (2/6).

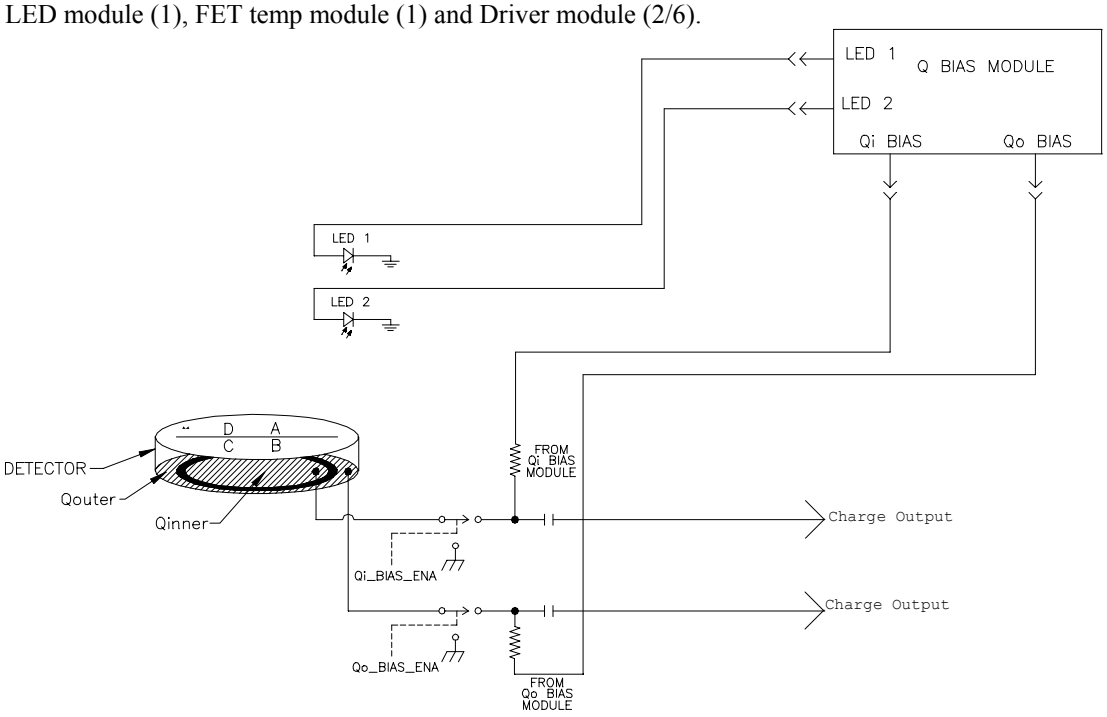


Figure 6: Charge Detector diagram

Charge Detector (Wayne Johnson, revised 6/02/99)
The detector crystal is either pure Germanium or pure Silicon, approximately 7.5 centimeters in diameter and one centimeter thick. The charge-collecting electrodes consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below.

Qbias Description (Tom Jankovsky, revised 6/07/99)
The Qbias module (schematic sheet 7-1) provides two DC bias voltage outputs (QI_Bias, QO_Bias) for supplying bias voltage to the detector charge collection segments, and two DC currents for flashing the trapped-charge-neutralizing LEDs (LED1, LED2) (schematic sheets 8-1 to 8-5). All four outputs are bipolar with an amplitude range of -5 to +5 Volts controlled via individual 12-bit DACs with a resolution of 2.44-millivolts per bit.

The bias voltages are connected to each of the two charge-collecting electrodes via a control relay. The control signal for the relays is QO_BIAS_ENA and QI_BIAS_ENA. When the bias voltage is enabled, the DAC output is connected to the signal line from the charge detector, when disabled, the signal line from the detector is connected to FEGND.

The other function of the Qbias module is to provide bias current for energizing the two trapped-charge-neutralizing LED's. For this purpose, the Qbias module has two current sources (U12 and U13 schematic sheet 8-1) using an INA105KU that are able to source, or sink, up to 5 milliamps, with 2.44-microamp/bit resolution. These two current sources are controlled independently, LED1_ENA and LED2_ENA, turning the current 'off' or 'on'. When 'on', the current can be turned on continuously, or pulsed. When pulsed

the output can either be a single pulse, or continuous stream of pulses. In the single pulse mode, the pulse width is adjustable via digital control, 10μSec to 100mSec. In the repetitive mode, both the pulse width (10μSec to 100mSec), and the pulse rate (1 pulse/mSec to 1 pulse/Sec), are adjustable via digital control.

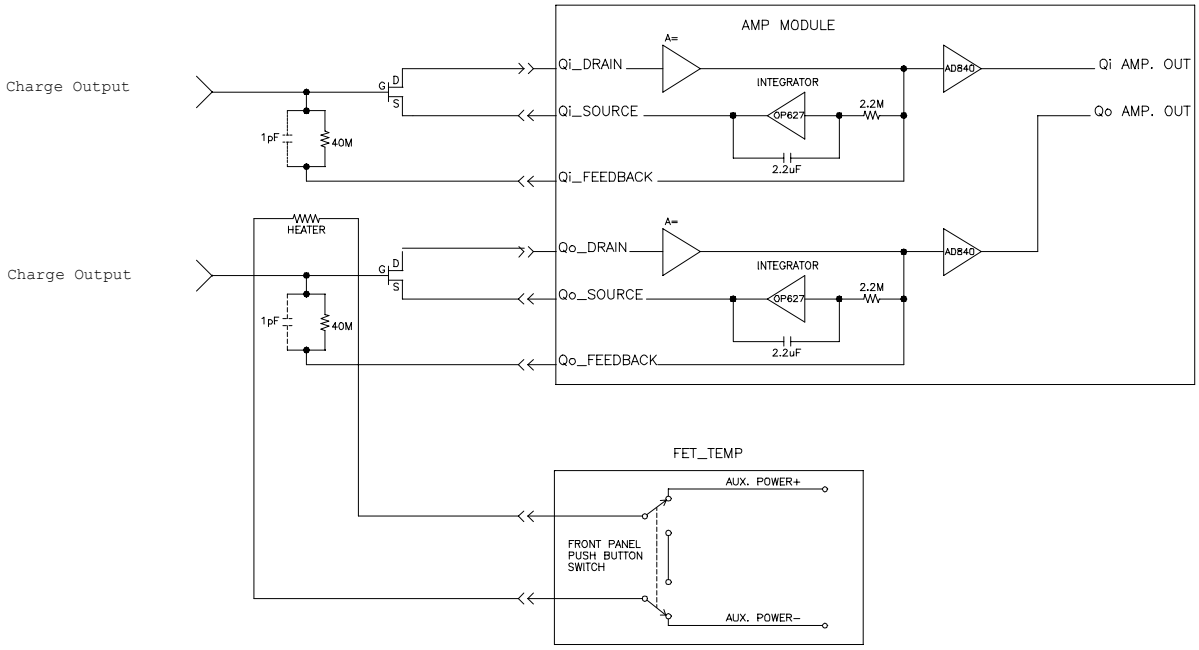
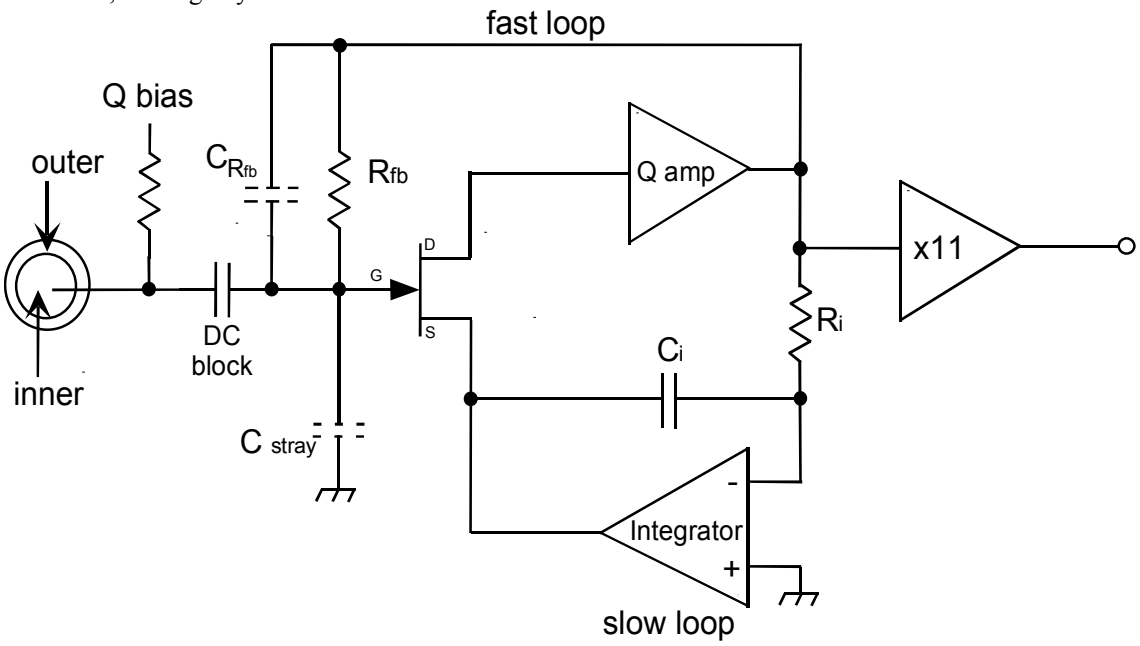


Figure 7: Q Amp and FET Temp Modules

Qamp Description (Merle Haldeman, Revised 5/21/99)
The Qamp module is used in conjunction with the front-end FET to convert charge collected from the detector to a voltage that ultimately gets sent to the data acquisition system for digitization. The detector has a disk shape, approximately 7.5 cm in diameter, and 1 cm thick. The charge collecting electrodes (two of them) consist of an outer ring and an inner disk on one surface of the semiconductor, as illustrated below. Although we only show the functional diagram for the inner electrode, a duplicate circuit is connected to the outer ring as well. The schematics for the Q amp are on Sheets 6-1 to 6-3.

A separate, individually controlled, DC bias voltage is provided to each of the charge-collecting electrodes (Q inner, Q outer) on the detector. The charge from each of the charge-collecting electrodes is AC coupled to a JFET-Gate through their respective DC Bias blocking capacitors. The JFET, being a voltage controlled device, is very sensitive to extraneous voltages at the gate node. Stray capacitance, C_{stray} , between the gate and it's surroundings is difficult to control and varies with mechanical vibrations. If a charge exists on C_{stray} due to a voltage difference between the JFET-Gate and its surroundings, then the changes in C_{stray} due to vibrations will cause corresponding changes in the voltage across C_{stray}, resulting in changes in voltage on the gate. This happens because the voltage on a capacitor is proportional to both capacitance (C) and charge (Q); V = Q/C; a change in either variable results in a change in voltage. If Q on C_{stray} is zero, then changes in C_{stray} due to mechanical variations, such as vibrations, will not produce corresponding changes in the voltage on the FET Gate. Also, reducing V to zero will make Q zero, and then the circuit will be independent of variations in C_{stray}.

The simplified theory of operation of the Q Amp is as follows. There are two feedback loops at work in this module (see the above illustration), a fast one and a slow one, both attempting to keep the FET Gate at zero volts, although by different methods.



Q AMP diagram

Slow loop:
Because the Fast loop DC couples the output of the Q Amp to the FET gate, and for the reasons previously stated, the FET Gate must be kept at zero volts, the function of the slow feedback path is to keep the output of the Q Amp at zero volts. It performs this function by integrating the voltage out of the Q Amp, and with an integrator having a time constant (RiCi) of 4.8 seconds, that applies this integrated output voltage to the source of the FET. As a result, the JFET remains biased at a point that keeps the output of the Q Amp at zero volts, by forcing the JFET-source positive, keeping the Gate-Source junction back-biased.

The actual operation of the slow loop is as follows. The typical, initial voltage levels are; the JFET-Gate is at ground voltage, Vgate=0V; the JFET-Source is at some positive voltage with respect to the JFET-Gate, possibly 3/4V and the JFET-Drain is at approximately three volts. The Q Amp output will equal zero volts when the JFET-Drain is at about 3 volts. The Q Amp is a non-inverting, high gain transconductance amplifier which provides about 15 volts at the output, per milliamp at the input. A decrease in the JFET-Drain current produces a more positive output voltage at the Q Amp output. This decrease in Drain current causes the inverting integrator to begin driving the JFET-Source in a more negative direction. This turns the FET on harder, causing a larger current flow in the JFET and thus an increase in the JFET-Drain current, opposing the original decrease

Fast loop:
The fast loop uses the fast signals created by the detector to keep the JFET-Gate near zero by neutralizing the charge injected into the gate node by the detector. This neutralizing charge is supplied from the output of the Q Amp through a parallel combination of a 40 Megohm resistor and it's approximately 1pF of parallel parasitic capacitance C_{Rfb}. This resistance and capacitance is called the **"Feedback Network"** of the fast loop. The amplitude of the Q Amp output pulse is determined by the capacitance in the feedback network and the quantity of charge from the detector, V=Q/C. Whatever charge passes through the DC Blocking capacitor, needs to pass through the C_{Rfb} in order the keep the gate at zero volts. For a given

charge, the output voltage is inversely proportional to the value of the Feedback Network capacitance, C_{Rfb}. The DC blocking capacitor situated between the Detector and the JFET-Gate blocks the bias voltage on the detector from affecting the JFET-Gate.

Both loops function to keep the JFET-Gate near zero volts.

Discrete Q Amp:
The basic design philosophy of the discrete amplifier is as follows. In order to minimize the effect of negative feedback (Miller effect), via the Drain-Gate parasitic capacitance, the Drain impedance is kept as low as possible. If the impedance were zero, then any changes in JFET Drain current would result in zero changes in Drain voltage and thus no negative feedback would result. Q_1 is a common-base, transimpedance amplifier, which provides a very low input impedance and a high output impedance. The input signal current is converted to a signal voltage across the collector load. The current gain is slightly less than one. Q_2 is a common collector stage having a very high input impedance and a very low output impedance. The high input impedance of second stage (Q_2) is required to keep the impedance of the collector load the first stage (Q_1) high. Q_2 has the low output impedance in order to be able to drive the cable going to the feedback resistor connected to the JFET-Gate. There is also an option to let Q_2 drive an intermediate, push-pull emitter follower amplifier made up of Q_3 and Q_4 (in the dotted line box on Sheet 6-2). This amplifier provides more drive capability, should the need exist. If there is no need for this amplifier, the components inside the dotted line-box may be left off the board and a jumper wire inserted at "S1".

FET Temp Description: (Steve Morrison)

This module supplies the signal, called variable (supplied from the backplane), used by the QET module's calibrate mode. There are two inputs to this module. A single ended or differential signal can be applied from a waveform generator through the floating front panel LEMO connector or a 10Hz signal can be received from the backplane. The output is a true differential signal to the backplane. It will be a buffered copy of either the signal to the front panel LEMO or the 10Hz from the backplane. A front panel switch selects which source is passed to the output. When the QET module is in calibrate mode, this signal is passed to the sensor bias.
This module contains 2 batteries that are used to supply current to the FET heater. The heater current is controlled by a momentary contact push-button-switch, which is mounted on the module's front panel.

Power Control Circuitry

Power control circuitry, version 1 (Wayne Johnson, revised 5/14/99)
The Zip Module can be powered by turning on the subrack power supply with the ZIP Module already plugged in. MOSFET transistors (Q1, Q2, Q3, Q4: IRF7416, IRF7413) are used as switches, to connect the fused, backplane supplied voltages, to the ZIP Module power planes. The MOSFET switches are controlled by the module power control circuitry. This circuitry utilizes a voltage monitor chip (U1B:MAX8216), a programmed sequencer chip (U104:CY37256P160-83AC) and the MOSFET drivers (U5B: PS2703-2).
The voltage monitor senses the voltages at the Module fuses. When all five of the voltages are at their proper levels, it enables the sequencer which starts the 4 Hz clock followed by sequentially turning on the MOSFET switches.
The backplane provides a 5-bit Local Address at each subrack slot, via pins P4-30-c, b, a, P4-29-b and a, for Local Address A0 through A4 respectively. In order to prevent all modules from powering-up simultaneously, with the associated high demand on the power supply, the time each ZIP Module power-on sequence starts is related to the Local Address of the module. The sequencer provides a delay for starting the power-on sequence based on the Local Address. The Local Address determines the number of clock ticks of the 4Hz clock that occur before the power-on sequence is begun. For example, slot 4 will have 4 clock pulses (1 second) of delay before starting the power-on sequence. The sequence order for turn on is

established by the user in the VHDL code that is programmed into the sequencer, Control Logic chip (U104). See ZIP LOGIC ADDRESSING section for an explanation of the code. Following the power-on sequence, the clock is disabled and the sequencer begins monitoring the output of the voltage monitor, the MOSFET switches are kept on while the voltage monitor output indicates all supplies are ok. When the voltage monitor output indicates a power supply problem all of the FET switches are turned off disconnecting the board voltage planes from the backplane supplied voltages. Figure 3 provides a functional block diagram of the power control circuitry.

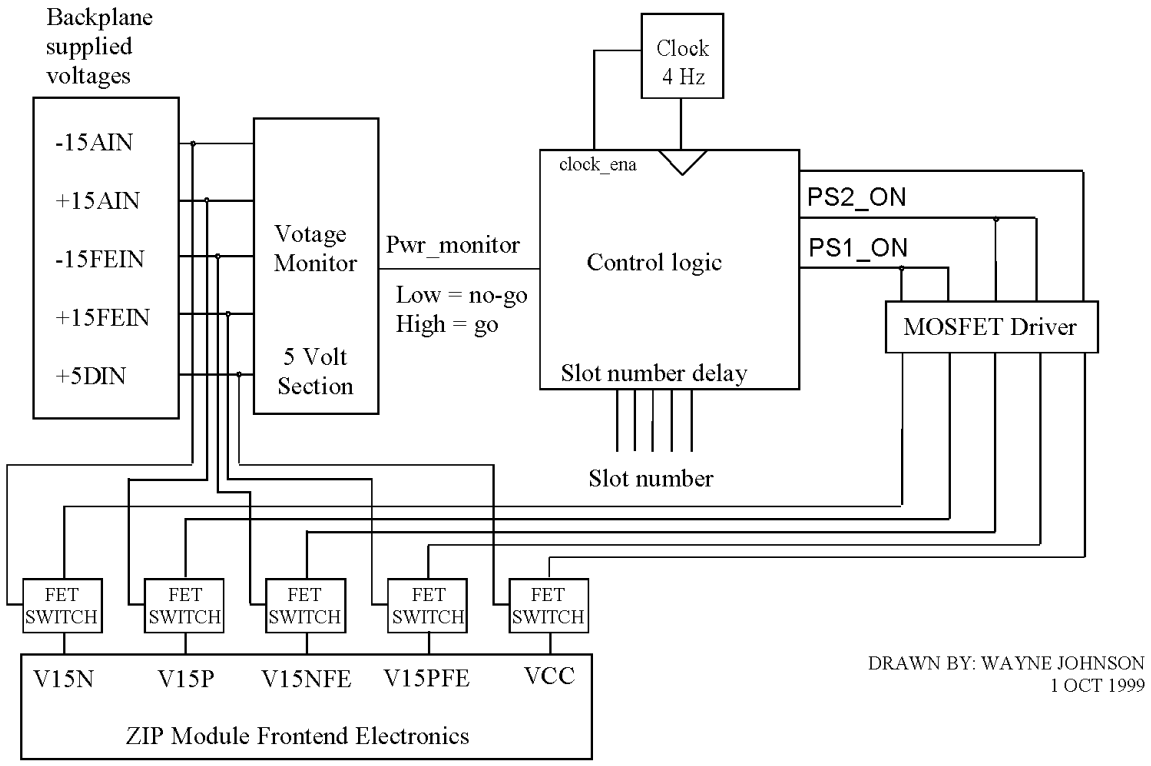


Figure 3: Power Control Circuit, Functional Block Diagram

Digital Interface (Wayne Johnson, revised Oct 7, 1999)

In order to appear as a single gate load to the crate backplane, all of the "address", "read", "write" and "data" lines are buffered. The address, read, and write buffers are unidirectional, always passing the backplane signals to the module, whereas the data buffers are bi-directional, with the direction being controlled by the read and write lines when the module is being addressed.

Hardware Busy Operation (Wayne Johnson, 10 April 2001)

The ZIP Version 2 module has been designed with a hardware busy control in the ZIPLogic chip. This busy signal prevents the receiving of any new 'Write' commands until the presently executing operation is done. This design was implemented to prevent the overlapping of commands since there is no handshaking capability between the board, gpib and controlling software. The problem was identified in modified version 1 boards when ZAP pulses were found to be missing during operational testing. The minimum delay associated with ALL commands is 80 mSec. This delay is the time allocated to the lighting of the front panel LED when the module is addressed. The longest delay is the 2 Sec delay for the ZAP pulse.

Table XXX: Module commands and the associated time delay.

CONTROL OUTPUT	TIMING DELAY	CONTROL OUTPUT	TIMING DELAY	CONTROL OUTPUT	TIMING DELAY

Squid Polarity outputs	
sq_pol_A_pos	80mSec
sq_pol_A_neg	80mSec
sq_pol_B_pos	80mSec
sq_pol_B_neg	80mSec
sq_pol_C_pos	80mSec
sq_pol_C_neg	80mSec
sq_pol_D_pos	80mSec
sq_pol_D_neg	80mSec

QET DAC/Test input	select
qetdac_ext_A	80mSec
qetdac_ext_B	80mSec
qetdac_ext_C	80mSec
qetdac_ext_D	80mSec

Charge Amp bias	enable
q_o_ena	80mSec
q_i_ena	80mSec

LED output enable	
led_1_ena	80mSec
led_2_ena	80mSec

Squid Integrator input	enable
ext_int_sq_A	80mSec
ext_int_sq_B	80mSec
ext_int_sq_C	80mSec
ext_int_sq_D	80mSec

External Test input	enable
test_ena_A	80mSec
test_ena_B	80mSec
test_ena_C	80mSec
test_ena_D	80mSec

Squid fb/pre integrator	mon
pre_int_mon_A	80mSec
pre_int_mon_B	80mSec
pre_int_mon_C	80mSec
pre_int_mon_D	80mSec

Squid Driver autozero	
ch_A_dao_ena	80mSec
ch_B_dao_ena	80mSec
ch_C_dao_ena	80mSec
ch_D_dao_ena	80mSec

Charge Amp autozero	
qo_dao_ena	80mSec
qi_dao_ena	80mSec

Heater Pulse outputs	
ena_heat_A	100mSec
ena_heat_B	100mSec
ena_heat_C	100mSec
ena_heat_D	100mSec

Zap Pulse outputs	
zap_ena_A	2 Sec
zap_ena_B	2 Sec
zap_ena_C	2 Sec
zap_ena_D	2 Sec

FET Heater turned ON	
fet_heat_on	80mSec

Software Reset of Board outputs	
system_reset	128mSec

Test Command	
test_pulse	80mSec

Enable bit w/Trig+/- for test pulse	
trig_ena	80mSec

Read Board information	
module_id	80mSec

Read/Write to Board	
module_select	80mSec

Charge Amp Gain outputs	
qo_gain_1	128mSec
qo_gain_10	128mSec
qo_gain_1_143	128mSec
qo_gain_2_5	128mSec
qo_gain_1_2	128mSec
qo_gain_143_5	128mSec
qo_pol_pos	128mSec
qo_pol_neg	128mSec
qi_gain_1	128mSec
qi_gain_10	128mSec
qi_gain_1_143	128mSec
qi_gain_2_5	128mSec
qi_gain_1_2	128mSec
qi_gain_143_5	128mSec
qi_pol_pos	128mSec
qi_pol_neg	128mSec

Squid Gain outputs	
chA_gain_1	128mSec
chA_gain_10	128mSec
chA_gain_1_143	128mSec
chA_gain_2_5	128mSec
chA_gain_1_2	128mSec
chA_gain_143_5	128mSec
chA_pol_pos	128mSec
chA_pol_neg	128mSec
chB_gain_1	128mSec
chB_gain_10	128mSec
chB_gain_1_143	128mSec
chB_gain_2_5	128mSec
chB_gain_1_2	128mSec
chB_gain_143_5	128mSec
chB_pol_pos	128mSec
chB_pol_neg	128mSec
chC_gain_1	128mSec
chC_gain_10	128mSec
chC_gain_1_143	128mSec
chC_gain_2_5	128mSec
chC_gain_1_2	128mSec
chC_gain_143_5	128mSec
chC_pol_pos	128mSec
chC_pol_neg	128mSec
chD_gain_1	128mSec
chD_gain_10	128mSec
chD_gain_1_143	128mSec
chD_gain_2_5	128mSec
chD_gain_1_2	128mSec
chD_gain_143_5	128mSec
chD_pol_pos	128mSec
chD_pol_neg	128mSec

DAC output setting

qet_daccs	80mSec
sq_bias_daccs	80mSec
sq_lockpt_daccs	80mSec
sq_gain_daccs	80mSec
sq_drv_daccs	80mSec
q_drv_daccs	80mSec
qbias_daccs	80mSec

NOTE:

Use this chart in conjunction with ZIPDECODING_V2.XLS for details about chip and addressing association.

ZIP Module ADDRESSING (Wayne Johnson, revised Oct 7, 1999)

The module addressing is done, utilizing four **C**omplex **P**rogrammable **L**ogic **D**evices(**CPLD**), each of which is programmed using **V**ery High Speed Integrated Circuit **H**ardware **D**efinition **L**anguage(**VHDL**). These four devices are divided into two groups; the first group consisting of a single device, and the second group consisting of the remaining three devices. The first group (CONTROL LOGIC, schematic sheet 13-3) decodes the Address Bits and the second group (CSR LOGIC, schematic sheet 13-4) decodes the Data Bits. Appendix B: Part 1:ZIP Section and Subsection Addresses is a table which shows the relationship between the sections, subsections and the Address bits whereas Part 2:ZIP CSR BIT Functions, is a table which lists the functions of the **C**ontrol and **S**tatus **R**egister(**CSR**) bits.

The first group decodes the Address bits in order to select the proper Subsection. If the subsection selected is a CSR(part of the second Group), then in the case of a write to the ZIP Module, whatever data is on the 16 bit Data Bus, is written to that CSR. In the case of a read, the data in that particular CSR is placed on the 16 bit Data Bus.

GROUP 1

Module Selection

Module selection is accomplished by comparing the five Address bits A12:A08(see Appendices A and B) on the Subrack address bus, to the five Local Address bits at the subrack slot, housing the ZIP Module. If these bits match during a read or write cycle, this module responds appropriately. The slot "Local Address is hard-wired into the subrack backplane, and are numbered from one on the extreme left (facing the front of the subrack) to twenty-one on the extreme right. The Control Logic chip (U104) on the ZIP Module compares the five Local Address bits with the five Address Bus bits A12:A08 to determine if the module is being addressed. If they match, the Module is selected and further decoding of the Section(A07:A04) and Subsection(A03:A00) is done. The Address Bus bit combinations for the subrack slot numbers are shown in Appendix B: Part 5.

Section Selection

The Control Logic chip (U104) determines the Section selected by decoding address bits A07:A04 allowing the user to address up to 16 possible sections. Appendix A: Shows the sections, and associated addresses, that are being utilized.

Subsection Selection

Subsection selection is accomplished by decoding Address bits A03:A00 again allowing the user to address up to 16 possible subsections. Appendix B-Part 2, shows the Function of the Data Bus bits for a given subsection.

When the Control Logic chip has determined that the ZIP Module has been selected and has decoded the section and subsection, in the event of a write cycle, an enable pulse is sent to the appropriate subsection chip to permit it to change board settings via the various CSRs, write values to the numerous DACs, Pulse the FET Heater or generate a Test Pulse.

Logic IC Decoded outputs
As can be observed from Appendix A and B, Part 1, there are four different types of Control Logic chip output signals decoded. They are Module information (Section 0), DAC selection (Sections 1, 2, 3, 4, 5, 6 and 7), CSR selection (Section E) and Test(Section F).

DAC Control Outputs (sections 1 through 5, subsections A through D, as well as sections 6 and 7, subsections 0 through 3)
DAC Control pulses select the addressed DAC to either be written to, or read from. Writing the DAC sets the analog voltage at the output of the DAC. Reading the DAC provides the last 12 bit word written to the DAC.

CSR Control Outputs (section E, subsections 0 through 5)
CSR Control outputs are pulses that select the addressed CSR for transfer of data buss information to the CSR (during a Write Cycle) or transfer of CSR data to the data bus (during a Read Cycle). The CSR subsections are listed in Appendices A and B-Part 2. Appendix B also provides the corresponding system parameter that each of the data bits controls.

Module Information(section 0, subsection 0)

Module Information is a read-only operation, which transfers a sixteen-bit-word containing the following module identification to the Data Buss for decoding: (See Appendix C)
1. Board serial number, (D07:D00)
2. Board version, (D11:D08)
3. Board type, (D15:D12)

Module identification bits are hard wired on the Module. The module's identification is set by connecting corresponding bits to +5V or ground.

Test Pulse(section F, subsection F)

Test Pulse can only be written to and has the following effects. write only control that is decodes 2 different output pulses. The first pulse, Test Pulse, is used to create an LED Pulse, a Zap Pulse or a Heat Pulse. The second pulse, FET Heater, is used to heat the FET in each of the two charge amplifier circuits. These FETs are mounted on the Squid Detector. Figure x shows the logic diagram on how the two pulses are decoded.

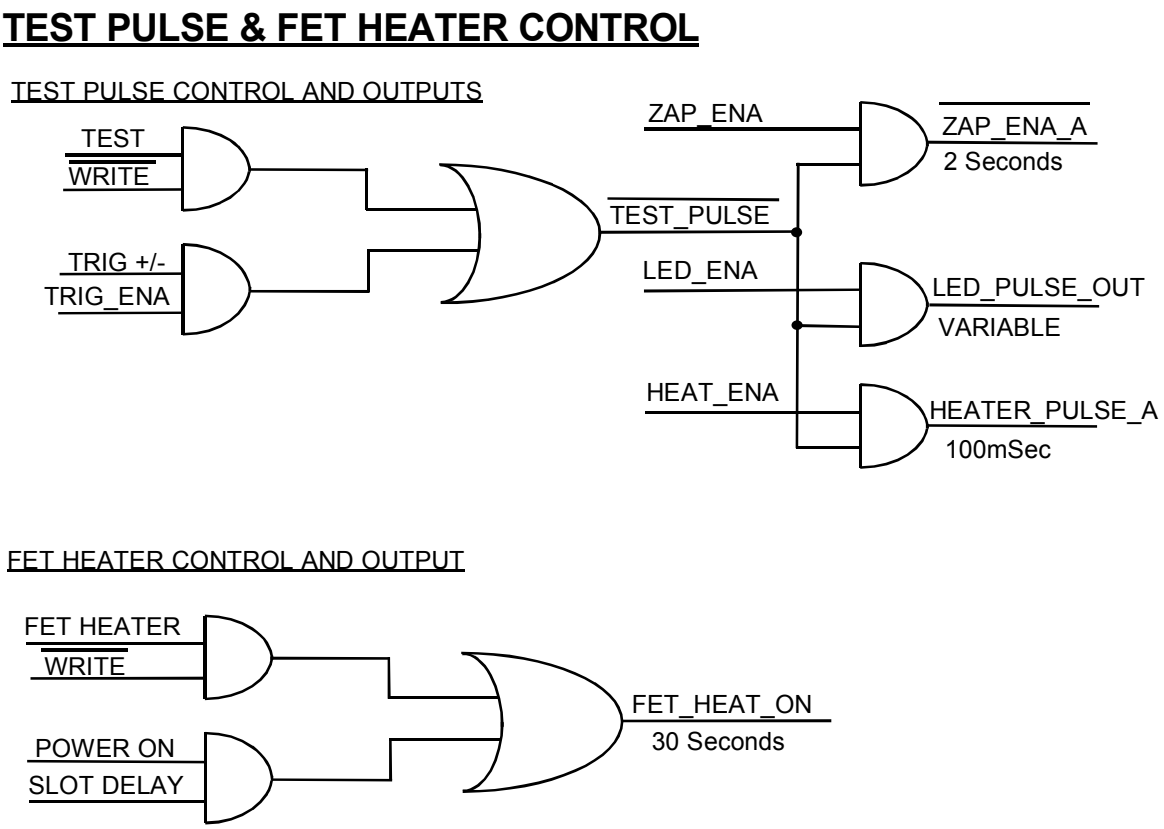


Figure 4: Test Pulse and Heater Logic

TEST_PULSE DECODING

The TEST_PULSE is developed in 2 ways.
1. The trig +/- signal, available at the backplane of the crate, is used in conjunction with the trig enable (trig_ena) command to develop TEST_PULSE in the coding of the CONTROL LOGIC chip. The signal, trig_ena, is bit 0 of CSR5 and when it is set high, it is enabled.
2. A write command to the Test Pulse address, xxFF, automatically produces a TEST_PULSE.

TEST_PULSE is an input into the CSR_LOGIC chips where the led pulse(s), heat pulse(s) and zap

pulse(s) are developed and outputted to the appropriate circuits. Which outputs get pulsed are dependent upon which of the output signals are enabled.

Group 2

This group of VHDL programmed chips handles the information on the data buss to set levels or toggle latching relays to enable the user to set board and system operating parameters. Chart 1 – Part 2 shows the CSR controls that are decoded by group 1 and the board signals that are set by the corresponding data bits when that CSR control is enabled.

Clocks

Clocks are used by some of the CSR subsections for incrementing counters. Each CPLD in Group 2 has a clock connected to an input. A clock is enabled when a CSR control input to the CPLD is enabled and disabled after all of the CSR's outputs have been sequenced through.

CSR outputs

There are two types of outputs generated when a CSR is enabled. They are either a latched output (ground, 5V) or a 5V pulse.

Latched output

The latched output is a permanent level that is set until changed to a different setting. See figure 1: latched output function diagram.

Pulsed output

The 5V pulse is used to toggle a latching relay. The duration of the pulse is 12mSec,long enough to ensure that the relay latches into the new setting. The pulse width is set by the clock speed and the number of clock pulses that the counter needs to count in order to equal the counter setting that is set in the VHDL code for each pulse type. See figure 2: sequenced, pulsed output function diagram.

The pulsed outputs are analyzed and sequenced so that only those relays that are changing state will be pulsed. The setting of the relay is compared to the new information that the CSR receives (wibd) and the present setting of the relay. The relay is pulsed if there is a change in setting, it is skipped if there is no change in setting. Relays that require pulses will be sequenced so that only one relay is pulsed at a time. This reduces the amplitude of the momentary current load that is caused by the activation of the relays.

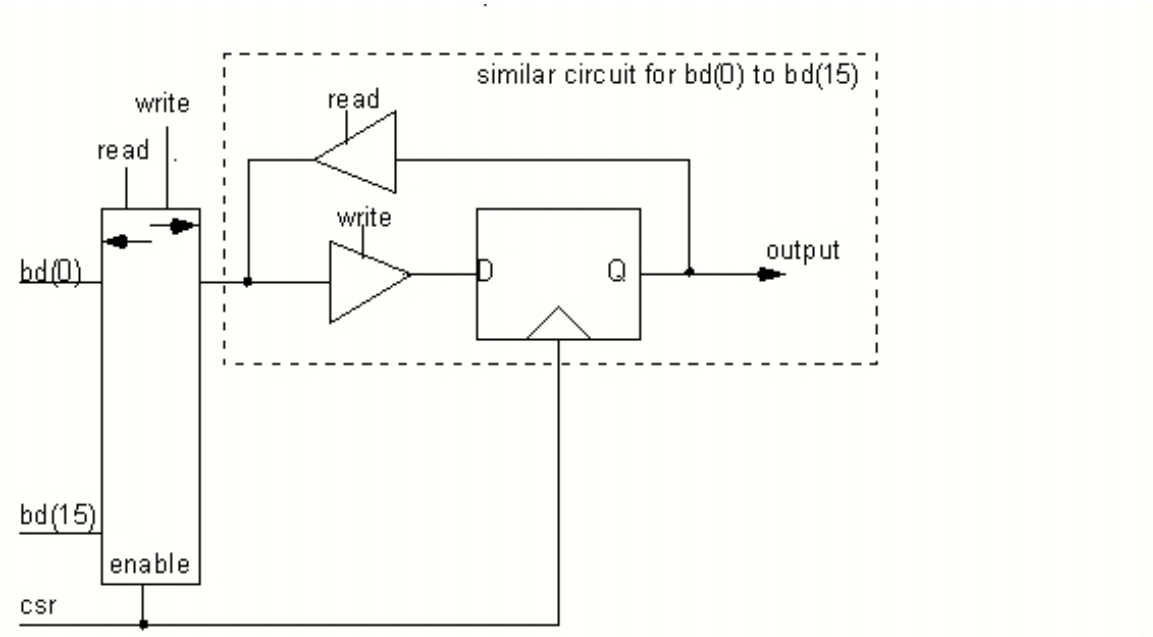


figure 2: latched output function diagram

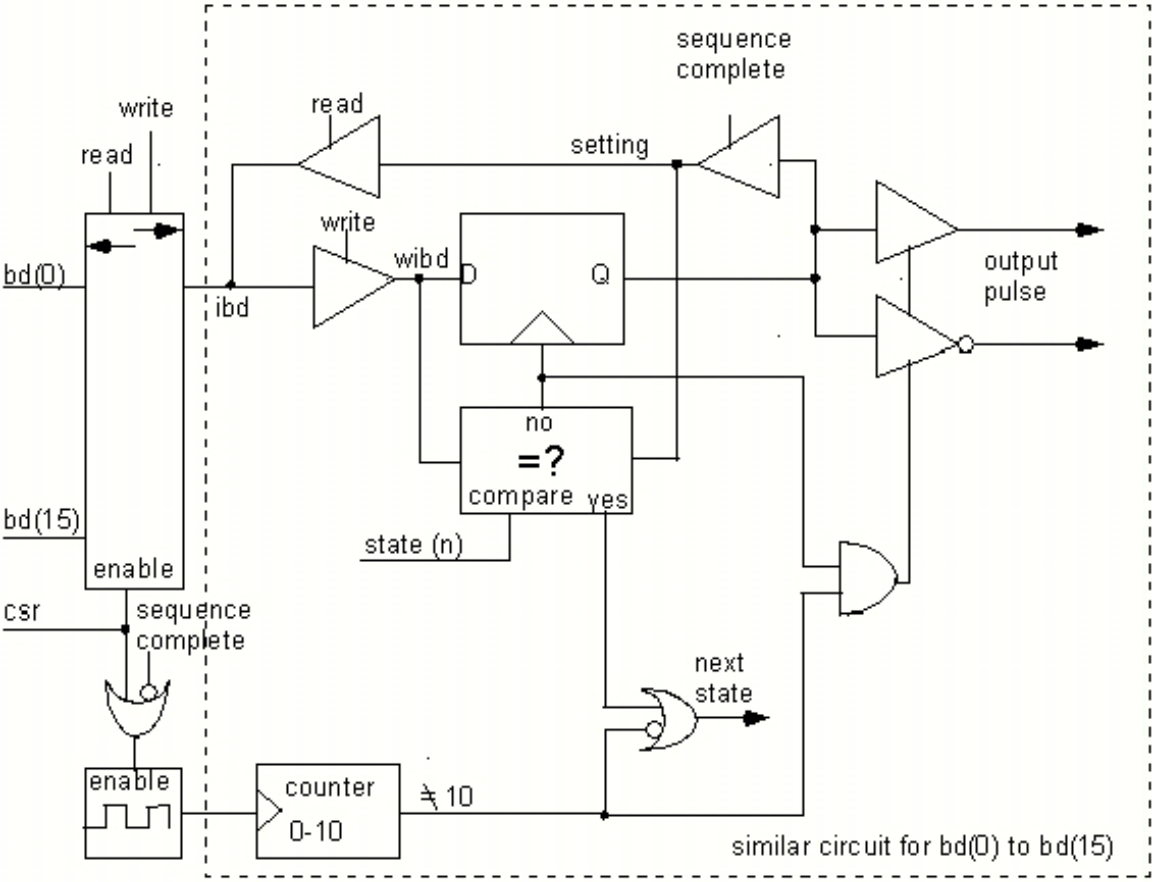


figure 3: sequenced, pulsed output function diagram

Digital To Analog Converters (DAC's) (Bruce Merkel ,revised 5/10/99)

There are seven, 12 bit, quad output DAC devices on this module, giving a total of 28 DAC outputs. Each DAC output has a range of +/- five volts, controllable in increments of approximately 2.44 millivolts / Bit. For each device, the four outputs are identified as 0, 1, 2 and 3. A 'system reset' will set the four outputs of each device to zero volts. The DAC output voltage is determined by the following formula, Vout = 5volts - (10/4096)N, where N is the binary code(in decimal) written to the DAC.

The QET portion of this 9U ZIP module uses all four outputs of the QET Bias DAC (U32). Each output controls the bias of one of the four QET sensors. Outputs 0, 1, 2 and 3 control sensors A, B, C and D respectively.

Each of the four SQUID electronics sections (A, B, C and D) of the ZIP module uses three DAC devices.
Squid Bias DAC (U34) outputs 0, 1, 2, and 3 go to the four squid front end sections A, B, C, and D respectively. This DAC is used to bias the SQUID at the most sensitive operating point.
The Squid Gain DAC (U36) outputs 0, 1, 2, and 3 go to the squid Variable Gain Amplifier section for squids A, B, C, and D. This DAC is used to control the second stage, voltage controlled, variable gain amplifier, with the DAC output voltage determining the gain, i.e., five volts out of the DAC sets the amplifier to a gain of 5.

The Squid LOCKPOINT DAC (U33) outputs 0, 1, 2, and 3 go to the squid front end and control the offset voltage of the first stage, (input amplifier). The +/- 5 volt output of the DAC translates to +/- 50 millivolts at the input to the first stage.

The ZIP board has six Driver channels, four to receive the four SQUID outputs, and two to receive the two Qamp outputs. Each Driver requires one DAC output to control it's input offset voltage.
The Squid Driver DAC (U31) outputs 0, 1, 2, and 3 go to their respective SQUID driver offset amplifiers A, B, C, and D.

The Qamp drivers utilize two of the Q Driver DAC (U37) outputs; 0: Qamp $_{Outer}$ and 1: Qamp $_{Inner}$. The other two outputs of Q Driver DAC are used for a test output (2) and a spare output (3).
The Q Bias DAC (U35) is used to control the Q(charge) Bias section of the ZIP module. The first two outputs (0, & 1) control Q-outer and Q-inner bias voltage, the second two outputs (2, & 3) control LED BIAS current magnitude and the ZAP DAC voltage.

Buffers (Bruce Merkel, revised 5/17/99)

The buffer is a unity gain amplifier used to translate signals referenced to Analog Ground (AGND), to signals referenced to Front End Ground (FEGND). The DAC outputs that are buffered are: Squid Bias, Squid Gain, Squid Lockpoint, QET Bias, Q_{inner} Bias and the Q_{outer} Bias. The Buffers are located at the place where the signal crosses over from the Analog Ground reference (AGND) to Front End Ground reference (FEGND). If a voltage difference exists between the grounds, the buffer acts to cancel that difference.
The output signal from the buffer (U1xx:LT1124CS8) is sent to a low pass filter with a 3dB roll off frequency of 13.5 Hz. The filter consists of a series resistor (R1xx: 4.99k) and a pair of Back to Back polarized capacitors (C1xx, C2xx). Two capacitors are needed in this configuration because the output of the buffer is bipolar.

References and Regulators (Bruce Merkel, revised 5/10/99)

The DAC Precision Voltage Reference AD588KQ (U1xx) generates a +/- 5 Volt reference which is used by the DAC +/-10 volt and DAC +/-5 volt regulators. The reference voltage comes into the positive input of a dual high speed precision OP-AMP LT1125S8 (U3xx). The output of the amplifier feeds the common pin of a 5 Volt regulator. Depending on the output voltage setting resistors on the regulator, the output voltage is either 10 or 5 volts. The +/- 10 Volt output is used by the DAC buffers, the DAC devices and

the Squid, Variable Gain Amplifiers. The +/- 5 Volt output is used by the DAC's and the –5 volt output is also used by the Squid Variable Gain Amplifiers and the QET Front End.

The Qamp 10 volt reference, is generated with a REF102AU (U6xx) and then buffered and filtered with an OPA27GU (U3xx) operating at unity gain. The buffered reference voltage is then supplied to the two 14 volt regulators which provide the +/- 14volts required to operate the two Q amplifiers. One amplifier for Q inner, and one amplifier for Q outer.

The 14 Volt regulators take the 10 volt buffered reference, and generate a separate +14 volts and –14 volts for each of the two Q amplifiers. OPA27GU (U5xx) regulates the + 14 volt output and OPA27GU (U4xx) regulates its –14 volt output.

The LM78L05 (U119) and the LM79L05 (U120) generate the +/-5QD voltages for the squid logic, from the Analog +/- 15 volts. The LM7805 (U122) and the LM7905 (U121) generates the +/-5Q voltage for the rest of the squid blocks from the Front End +/- 15 volts.

The MIC5206-5.0BMM (U126) generates a low noise 5 volts for the LED Driver, QBIAS_FE and the QET SELECTOR from the Front End +15 volts.

Zip Module LED Current Control (Tom Jankovsky, Revised 5/25/99)

The LED Current Control contains four analogue switches (U1), which are flipped in response to signals from the LED Pulse Control. These input signals include *LED1ENA*, *LED1PULSE*, *LED2ENA*, and *LED2PULSE*. The two enables(*ENA*), connect the output of the controlling DAC to the input of the appropriate Current Source. The two pulse(*PULSE*) inputs control the switches which are connected in parallel with the LED's which either pass the current source output to Front-end Ground(FEGND) or cause it to be forced through the LED. A separate input signal, LED_BIAS, supplied from the DAC section, contains the required voltage for setting the magnitude of current from the voltage controlled current source. The following is a truth table for the switches:

SWITCH	TYPE	INPUT PIN	OUTPUT PIN	CONTROL PIN	CONTROL INPUT	SWITCH POSITION
1	N.O.	6	7	8	0	OPEN
2	N.C.	11	10	9	0	CLOSED
3	N.O.	3	2	1	0	OPEN
4	N.C.	14	15	16	0	CLOSED

SWITCH ONE connects input signal from the DAC, *LED_BIAS*, to the output signal, *LED_BIAS_1*, when a HIGH is placed on *LED1ENA* (pin 8 of U1). The output signal, LED_BIAS_1, is then sent to the input of the LED Current Source section.
SWITCH TWO connects the output signal, *LED1*, to front-end ground (*FEGND*), when a LOW is placed on *LED1PULSE*.
SWITCH THREE connects input signal, *LED_BIAS*, to the output signal, *LED_BIAS_2*, when a HIGH is placed on *LEDENA2*. The output signal, *LED_BIAS_2*, is then sent to the input of the LED Current Source section.
SWITCH FOUR connects the output signal, *LED2*, to front-end ground (*FEGND*), when a LOW is placed on *LED2PULSE*.

The output signals, LED_BIAS_1, LED1, LED_BIAS_1, and LED2 are sent to the Current Control section.

Zip Module LED Current Source (Tom Jankovsky, Revised 5/25/99)

The LED Current Source section provides current to the Led, corresponding to an input voltage from *LED_BIAS*. This section is designed as a differential input voltage-to-current converter, because LED luminosity is proportional to the current through it. The input voltage line, *LED_BIAS*, comes from the DAC section and enters pin 3 of a precision, unity-gain, differential amplifier (U5). The other input of this amplifier, pin 2, is tied to analog ground. Since the amplifier is configured differentially, the output voltage at pin 6, with respect to pin 1, will be the voltage difference between pins 2 and 3. =

$V_{pin6} - V_{pin1} = V_{pin3} - V_{pin2}$

V_{pin2} is connected to analog ground (AGND) and so it can be considered zero. The formula simplifies to:

$V_{pin6} - V_{pin1} = V_{pin3}$ which is the DAC output voltage.

But $V_{pin6} - V_{pin1}$ is the voltage across R_{18}, resulting in the current through R_{18} being very close to V_{pin3}/R_{18}.l This is the current sent to the LED. In our case, R (R18) is 1.0K. As the LED becomes brighter, the dynamic resistance of it changes. The op-amp (U3: OPA627GU) eliminates this voltage drop by maintaining a potential of zero across both of its inputs. The voltage controlled current source gives us the ability to know how much current flows through the LED, and thus the luminosity, just by setting the DAC voltage.

The Led Current Source will only drive the LED for short bursts of time to neutralize trapped charges in the detector crystal. The amplifiers in this circuit have relatively slow transient responses, and so are operated in a DC mode with the DAC controlling the magnitude. The higher-speed analog switches (U1: DG413DY) of the Current Control section carries out the switching of the output signal *LED1*. To stop the current from entering the LED, the analog switch closes, sending the current to front-end ground. When the analog switch opens current flows from the output line, *LED1*, to the LED.

Zip Module LED Pulse Control (Tom Jankovsky, Revised 5/25/99)

The purpose of the LED Pulse Control section (schematic sheet 8-3), is to decode lines for the LED Current Control section. The LED Pulse Control section receives control signals from the CSR Logic section on lines *LED1_ENA*, *LED_PULSE_OUT*, and *LED2_ENA*. Lines *LED1_ENA* and *LED2_ENA* are enabling lines while *LED_PULSE* is the pulsed control line. The logic of this section ANDs *LED1_ENA* with *LED_PULSE* to create the output signal, *LED1PULSE*. The logic also ANDs *LED2_ENA* with *LED_PULSE* to create another output signal, *LED2PULSE*. The *LED1PULSE* output signal operates by first setting *LED1_ENA* HIGH, and then pulsing *LED_PULSE* for the required duration. The *LED2PULSE* output signal operates by first setting *LED2_ENA HIGH*, and then pulsing LED_PULSE for the required duration. The input signal, *LED1_ENA* is passed through to the output *LED1ENA*. The same is true for the output signal, *LED2ENA*. Both output signals contain a 10K current limiting resistor to protect the CSR logic chip, as well as the AND gates from short circuits as well as providing some low-pass filtering for the signals on the way to the analog switches. After passing through the resistors, these four signals are used as the analog switch control lines in the LED Current Control section.

Zip Module External Test Receiver (Steve Morrison, Revised 5/21/99)

The external test receiver section is a unity gain amplifier which converts a differential signal, received from the backplane via the 48 pin connector, to a single-ended signal referenced to front-end ground. Voltage differences between the inputs and front end ground are rejected by the amplifier. The low-pass filtered signal is then sent to the QET bias section, which when operated in the calibrate mode, sends this signal to it`s "A,B,C, or D Bias" outputs.

Specifications:

Power:

This module utilizes the following voltages and requires the indicated currents capability.

Voltage	Typical current	Maximum current	*Inrush Current
+15 FE	0.570 Amperes	0.700 Amperes	1.0 Amperes
-15 FE	0.510 Amperes	0.700 Amperes	0.7 Amperes
+15 A	0.350 Amperes	0.400 Amperes	1.8 Amperes
- 15 A	0.350 Amperes	0.400 Amperes	0.4 Amperes
+5	0.500 Amperes	0.600 Amperes	0.8 Amperes

This produces a total power dissipation of 29.2 Watts.

Some internal voltages and their typical respective loads are as follows:

+5Q	0.463 Amperes
-5Q	0.360 Amperes

* Inrush current occurs when power is initially applied to the module.

Bandwidth:

SQUID:

The frequency response of the SQUID electronics, from input to feedback, is as follows:

Variable gain amp setting	Channel gain @ 1kHz	Upper 3dB frequency
0.5	574	2.4kHz
1.0	1150	2.4kHz
2.5	2870	2.4kHz
5.0	5740	2.4kHz
10	11500	2.4kHz
25	28700	2.4kHz
50	57400	2.4kHz

Driver:

The frequency response of the DRIVER circuitry, from input to output, is as follows:

Driver gain setting	Driver gain @ 100kHz	Upper 3dB frequency
1.0	1	1.0MHz
1.43	1.43	1.0MHz
2.0	2.0	1.0MHz
5.0	5.0	1.0MHz
10	10	1.0MHz
14.3	14.3	1.0MHz
20	20	1.0MHz
50	50	1.0MHz

Note: Allow at least 120 milliseconds between commands issued to modify a Driver channel gain.

Noise:

SQUID

The noise produced by the SQUID electronics, from input to feedback, is as follows:

Variable gain amp setting	Channel gain @ 1kHz	Noise in nV/Rt-Hz 100Hz	200Hz	500Hz	1kHz	2kHz
0.5	574					
1.0	1150					
2.5	2870					
5.0	5740					
10	11500					
25	28700					
50	57400					

QET Bias

The noise produced by the QET Bias electronics output, is 4 nV/Rt-Hz from 100Hz up.

Q Bias

The noise produced by the Q Bias electronics output, is 4 nV/Rt-Hz from 100Hz up.

SQUID Bias

The noise produced by the SQUID Bias electronics output, is 4 nV/Rt-Hz from 100Hz up.

Appendix A; (Wayne Johnson; Revised 9/15/99)

A trig +/- signal, available at the backplane of the crate, is used in conjunction with the trig enable(trig_ena) command, to develop a zippulse in the coding of the CSR chips. A zippulse executes the following outputs: led pulse(s), heat pulse(s) and/or zap pulse(s). Which outputs get pulsed are dependent upon which of the output signals are enabled. trig_ena is bit 0 of CSR5 and when it's set to 1 (high), it is enabled.
The following is a copy of how the code is written and what it does:

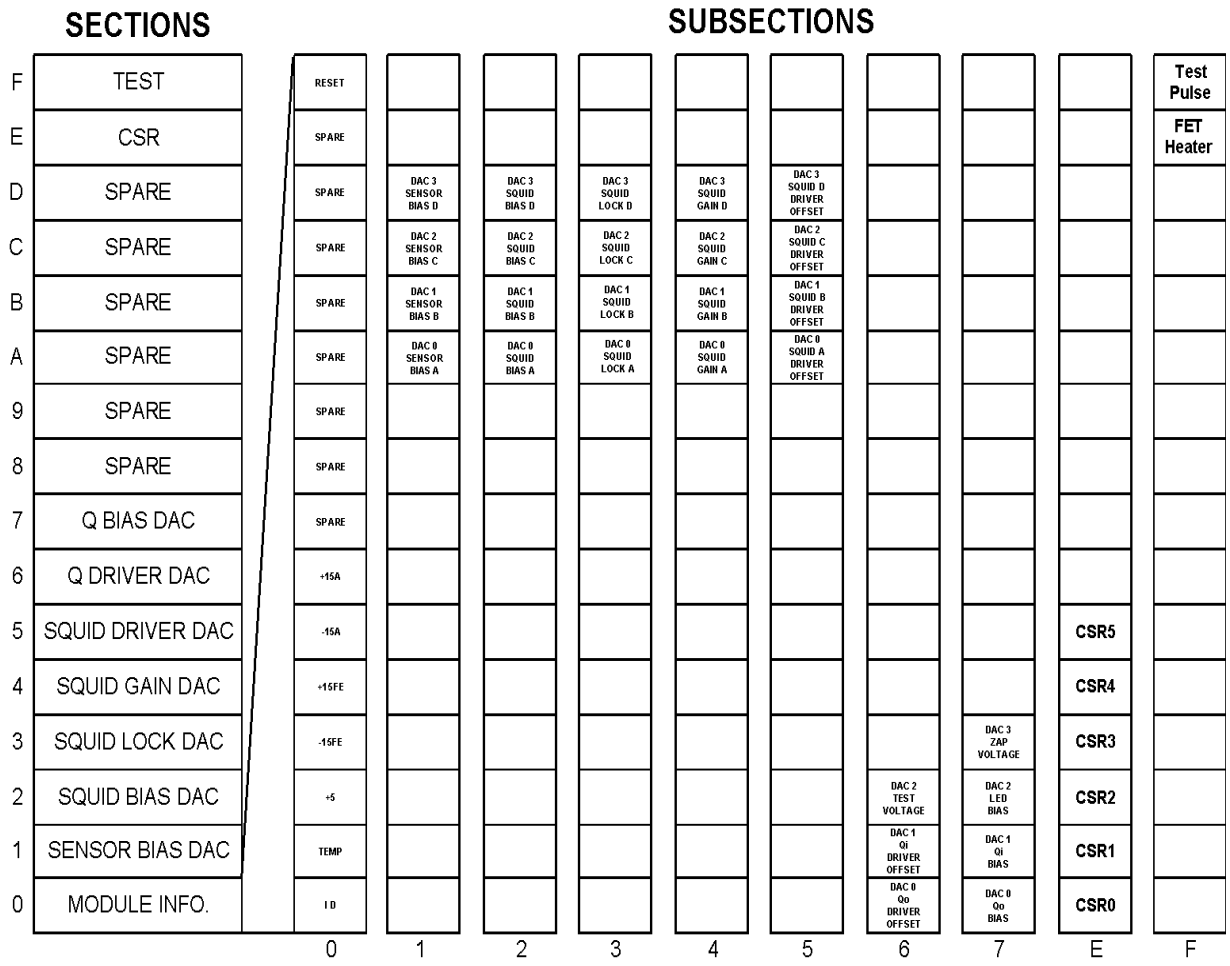
```
zippulse <= '1' when (write='0' and testpulse='0') or (trigplus_minus='1' and trig_ena='1') else
        '0' when clock='1';

ledpulse: process(clock, zippulse) note: this initiates the led pulse
        begin
                if rising_edge(clock) then
                if zippulse='1' then

zappulse: process(zippulse, clock) note: this initiates the zap pulse
        begin
                if rising_edge(clock) then
                if zippulse='1' then
                heaterpulse: process(zippulse, clock) note: this initiates the heat pulse
        begin
                if rising_edge(clock) then
                if zippulse='1' then
```

Appendix A1; (ZIP Module Addressing)

ZIP MODULE ADDRESSING

UNUSED			Subrack SLOT					SECTION				SUBSECTION			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Available for possible future addition



Notes:

1. For addressing purposes, modules are divided into 16 sections, each having a 4 bit address. Each section is divided into 16 subsections. For example, in order to address the FET Heater of a ZIP Module plugged into Subrack-SLOT 7, you would use address 0011111111110; or hexadecimal address 07FE

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Revised 9/27/99

Appendix B; (Wayne Johnson; Revised 5/10/01) Taken from ZIPDECODING_v2.XLS

		PART 1: SECTION, SUBSECTION DECODING		
SECTION	**SUBSECTION**	SUBSECTION	section/subsection	
DAC/CSR name	DAC/CSR	NAME	address	section decoding
Module Info	ID		xx00	zip logic
section 0	RESET		xx0F	zip logic
QET DAC	DAC 0	Sensor Bias A	xx1A	zip logic
section 1	DAC 1	Sensor Bias B	xx1B	zip logic
	DAC 2	Sensor Bias C	xx1C	zip logic
	DAC 3	Sensor Bias D	xx1D	zip logic
Squid Bias DAC	DAC 0	Squid Bias A	xx2A	zip logic
section 2	DAC 1	Squid Bias B	xx2B	zip logic
	DAC 2	Squid Bias C	xx2C	zip logic
	DAC 3	Squid Bias D	xx2D	zip logic
Squid Lock DAC	DAC 0	Squid Lock A	xx3A	zip logic
section 3	DAC 1	Squid Lock B	xx3B	zip logic
	DAC 2	Squid Lock C	xx3C	zip logic
	DAC 3	Squid Lock D	xx3D	zip logic
Squid Gain DAC	DAC 0	Squid Gain A	xx4A	zip logic
section 4	DAC 1	Squid Gain B	xx4B	zip logic
	DAC 2	Squid Gain C	xx4C	zip logic
	DAC 3	Squid Gain D	xx4D	zip logic
Squid Driver DAC	DAC 0	Squid Driver A	xx5A	zip logic
section 5	DAC 1	Squid Driver B	xx5B	zip logic
	DAC 2	Squid Driver C	xx5C	zip logic
	DAC 3	Squid Driver D	xx5D	zip logic
Q Driver DAC	DAC 0	Q O Driver	xx60	zip logic
section 6	DAC 1	Q I Driver	xx61	zip logic
	DAC 2	Test Voltage	xx62	zip logic
	DAC 3			zip logic
Q Bias DAC	DAC 0	Q O Bias	xx70	zip logic
section 7	DAC 1	Q I Bias	xx71	zip logic
	DAC 2	LED Bias	xx72	zip logic
	DAC 3	Zap Voltage	xx73	zip logic
unused section 8 to D				
CSR	CSR0	QET CSR	xxE0	zip logic
section E	CSR1	Squid CSR	xxE1	zip logic
	CSR2	Squid Driver CSR	xxE2	zip logic
	CSR3	LED CSR	xxE3	zip logic
	CSR4	Q CSR	xxE4	zip logic
	CSR5	CSR5	xxE5	zip logic
Test		Test Pulse	xxFF	zip logic
section F		FET Heater	xxFE	zip logic
The Module is decoded from bits 8 to12 of the address bus	The SECTION is decoded from bits 4 to 7 of the address bus	The SUBSECTION is decoded from bits 0 to 3 of the address bus		Outputs are from logic #1: zip_logic3.vhd

PART 2: CSR SUBSECTION OUTPUTS vs DATA BUSS BITS

Data Bit	QET CSR	Squid CSR	Squid Driver CSR	LED CSR	Q CSR	CSR5	Module ID
BD0	***QET_DAC_EXT_A***	***EXT_INT_SQ_A***	**CHA_GAIN0**	WIDTH_0	***Q_O_GAIN0***	TRIG_ENA	Serial Number bit 0
BD1	***QET_DAC_EXT_B***	***EXT_INT_SQ_B***	**CHA_GAIN1**	WIDTH_1	***Q_O_GAIN1***		Serial Number bit 1
BD2	***QET_DAC_EXT_C***	***EXT_INT_SQ_C***	**CHA_GAIN2**	WIDTH_2	***Q_O_GAIN2***		Serial Number bit 2
BD3	***QET_DAC_EXT_D***	***EXT_INT_SQ_D***	**CHA_POLARITY**	WIDTH_3	***Q_O_POLARITY***		Serial Number bit 3
BD4	***QET_ENA_HEAT_A***	***SQ_POL_A_-***	**CHB_GAIN0**	WIDTH_4	***Q_I_GAIN0***	CH_A_DAO_ENA	Serial Number bit 4
BD5	***QET_ENA_HEAT_B***	***SQ_POL_B_-***	**CHB_GAIN1**	WIDTH_5	***Q_I_GAIN1***	CH_B_DAO_ENA	Serial Number bit 5
BD6	***QET_ENA_HEAT_C***	***SQ_POL_C_-***	**CHB_GAIN2**	WIDTH_6	***Q_I_GAIN2***	CH_C_DAO_ENA	Serial Number bit 6
BD7	***QET_ENA_HEAT_D***	***SQ_POL_D_-***	**CHB_POLARITY**	WIDTH_7	***Q_I_POLARITY***	CH_D_DAO_ENA	Serial Number bit 7
BD8		TEST_ENA_A	**CHC_GAIN0**	RATE_0	Q_O_ENA		Board Version bit 0
BD9		TEST_ENA_B	**CHC_GAIN1**	RATE_1	Q_I_ENA		Board Version bit 1
BD10		TEST_ENA_C	**CHC_GAIN2**	RATE_2	Q_O_DAO_ENA		Board Version bit 2
BD11		TEST_ENA_D	**CHC_POLARITY**	RATE_3	Q_I_DAO_ENA		Board Version bit 3
BD12	***ZAP_ENA_A***	PRE_INT_MON_A	**CHD_GAIN0**	RATE_4	LED_1_ENA		Board Type bit 0
BD13	***ZAP_ENA_B***	PRE_INT_MON_B	**CHD_GAIN1**	RATE_5	LED_2_ENA		Board Type bit 1
BD14	***ZAP_ENA_C***	PRE_INT_MON_C	**CHD_GAIN2**	RATE_6	LED_CTRL_0		Board Type bit 2
BD15	***ZAP_ENA_D***	PRE_INT_MON_D	**CHD_POLARITY**	RATE_7	LED_CTRL_1		Board Type bit 3

Register outputs that are PLAIN text are outputs of the latching register: logic #2: csr_logic3.vhd

Register outputs that are BOLD text are outputs that are pulses from logic #3: ziprelay2.vhd

Register outputs that are bold and italized text are outputs that are pulses from logic #4: chargeamps.vhd

Module Info ID bits are read only. These are shorts to +VCC or GND to set the condition

PART 3: GAIN AND POLARITY DECODING MATRIZ

Data bits to the DACs set the output voltage level

DAC output voltage calculation:
Vout=Vrefl +((Vrefh-Vrefl) * N)/4096
N= is digital code in decimal

POLARITY	2	1	0	GAIN
0	0	0	0	1
0	0	0	1	1.43
0	0	1	0	2
0	0	1	1	5
0	1	0	0	10
0	1	0	1	14.3
0	1	1	0	20
0	1	1	1	50
1	0	0	0	-1
1	0	0	1	-1.43
1	0	1	0	-2
1	0	1	1	-5
1	1	0	0	-10
1	1	0	1	-14.3
1	1	1	0	-20
1	1	1	1	-50

NOTE:
ALL SIGNAL NAMES ARE HIGH TRUE

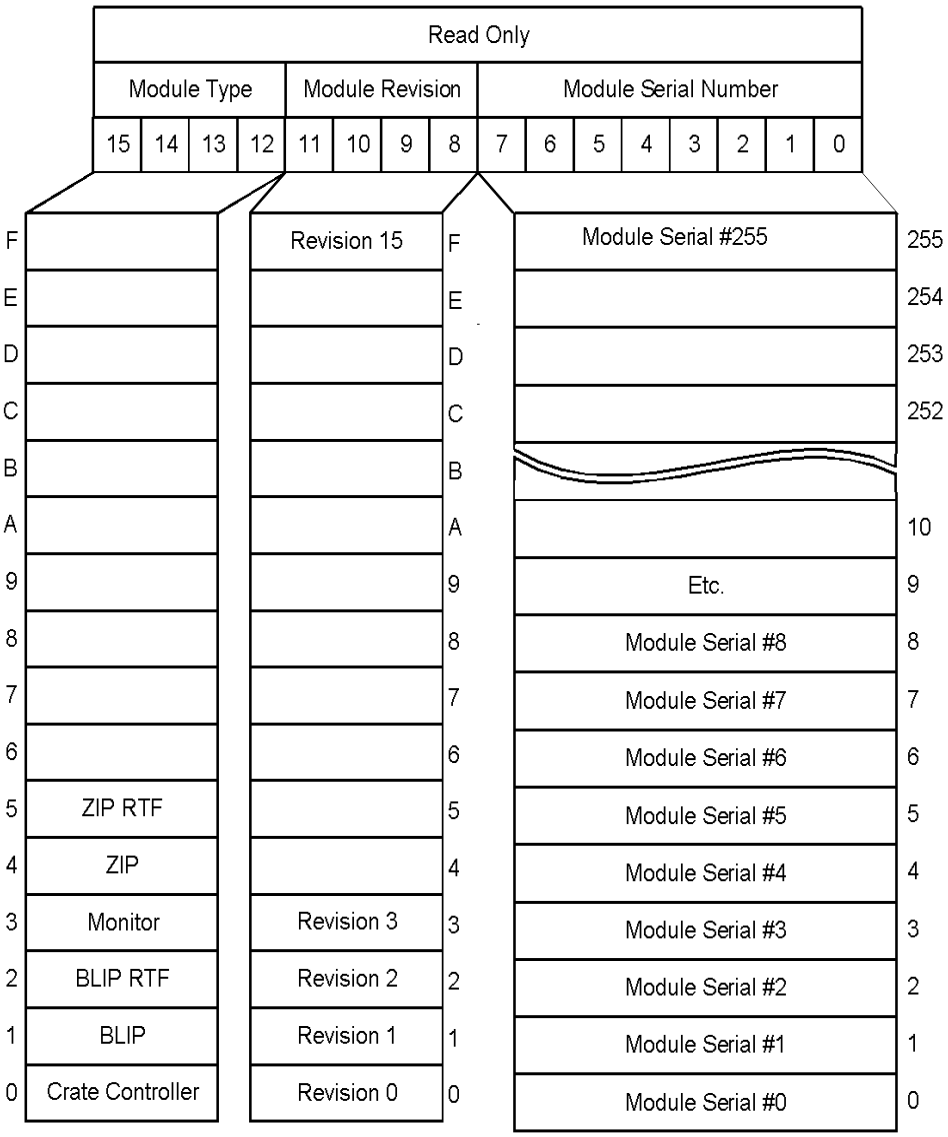
LED_CTRL_1	LED_CTRL_0	
0	0	OFF
0	1	SINGLE
1	0	MULTI
1	1	ON

Appendix C; (Module Identification)

CDMS(E-891) Module Identification Explanation

This file is named MODULE_ID.CV5 and is located at

Network Neighborhood\Entire Network\Microsoft Windows Network\Fnal\
Ppdserver1\ETT.PPD\Projects\Ett_ES\Cdms\module\9U\geneeral\Identification



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Revised 05/19/99

Appendix D; (Module Logic Section Notes)

Note 1: Logic busy upgrade implemented into module addressing control. The busy upgrade prevents the user from sending multiple ‘write’ commands to the module while it is in the process of completing a ‘write’ operation. This control only applies when writing to the ‘Squiddriver’ and ‘Chargeamp’ chips which have a minimum timing loop of 128 mSec to cycle through the latching relays that are used for Driver Gains. The busy signal is feedback from the chips to the ‘Zip_logic’ chip, which decodes the module address and ‘read’ or ‘write’ operation. The combination of the busy signals and ‘write’ prevent the acceptance of a ‘write’ operation until the chip says it is no longer busy. This upgrade does not prevent a ‘read’ operation of any part of the logic while a ‘write’ operation is being executed.

Note 2: Read operation of Driver Gains. Attempting to do a ‘read’ operation on the Driver Gains while the gains are being set will result in an incorrect reading if the specific channel being ‘read’ is being changed. The CPLD responsible for the addressed gain does not change the intermediate data bit, which is ‘read’ out to the user, until after all of the bits have been processed, this operation takes approximately 127 mSec.